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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	**Application No.** 10/822,115	**Applicant(s)** STOLOWITZ, MICHAEL C.	
	Examiner YAIMA CAMPOS	**Art Unit** 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/822,115, the examiner acknowledges the applicant's submission of the amendment dated 7/29/2010. At this point, claims 1, 10, 17 and 26 have been amended. Claims 1-31 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 2/17/2010 has been entered.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8-12, 14-17, and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186) in view of Stolowitz (US 6,018,778).

As for claims 1 and 10, Searby teaches a method of reading stored data from an array of independent disk drives so as to provide synchronous data transfer into a buffer, the method comprising:

for each disk drive in the redundant array (Fig. 2 elements 21-24), providing a corresponding FIFO/two-port memory (col. 8, lines 2-6 – RAM buffers (Fig. 2, elements 37-40 are dual port in nature)) for receiving and storing read data responsive to timing signals provided by the respective drive (col. 3, lines 52-67). Also note since data is written in and out sequentially (i.e. the buffers are used to "buffer" data streamed sequentially – i.e. video data - col. 1, lines 7-29), hence the buffer RAMs act as FIFOs;

initiating a READ command to each of the drives of the array, thereby causing each of the drives to retrieve selected elements of its stored data, and to transfer the retrieved data from the drive into its corresponding FIFO/two-port memory using the timing signals provided by the respective drive<u>, wherein for each of the drives, the drive provides one of the timing signals according to which the retrieved data is transferred from the drive into the drive's corresponding two-port memory;</u> (With respect to this limitation, Searby discloses col. 5, lines 38-49; col. 7, lines 12-26 – the control bus is used to in conjunction with request signals (REQ) to indicated a READ command – i.e. when data is to be read from the drives to the RAM buffers, and explains "individual sub-controllers… between each of the second SCSI interfaces 33 and 36 and their respective RAM buffer 37 to 40. Each sub-controller would monitor the request signal REQ from its second SCSI interface and in response to a request would strobe the write line of its RAM buffer causing a word to be transferred from the second SCSI interface to the RAM

buffer" (col. 7, lines 14-20), describing the embodiment depicted in fig. 2 as "disc drives and associated circuitry" (col. 7, lines 60-61); *where Applicant should note that SCSIs and the disclosed sub-controllers are associated with each of the disk drives and may thus be interpreted as forming part of the disk drives (Refer to Board decision, page 11, lines 1-12); therefore, having the disk drives provide the timing signals. Further, it would have been obvious to one having ordinary skill in the art to place the disk and associated circuitry (i.e., SCSI and sub-controller) as disclosed by Searby within the same chip or drive, since relocation or rearrangement of parts is an obvious matter to one having ordinary skill in the art. In re Japikse,* 86 USPQ 70);

monitoring each of the FIFO/two-port memories to detect a non-empty condition (col. 7, lines 32-46 – the system transfers the data to the data highway (Fig. 2, element 49) based on the determination that data is stored in the RAM buffers. Since all the buffers receive data substantially concurrently (i.e. all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e. non-empty condition), or not present. Data present in the RAM buffers is an implied acknowledgment that data have been received from the disk stores. Note the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur); and

waiting until all of the FIFO/two-port memories indicate such a non-empty condition; then synchronously reading the transferred data from all of the FIFO/two-port memories, thereby forming synchronous read data, and writing the synchronous read data

into the buffer (col. 7,lines 32-35 – once all RAMs indicate a non-empty condition (i.e. data is present in each RAM), the data is sent to the data highway and subsequently to the register (i.e. buffer) as shown in Fig. 2, element 50 (see also col. 5, lines 22-37 and col. 6, lines 14-31)). Again, the RAM buffers store data such that either all contain data, or no buffers contain data, therefore the data cannot be transferred until all RAM buffers have data (i.e. are non-empty); and

repeating said monitoring, waiting; reading and writing into the buffer steps until completion of a read operation initiated by the said READ command (col. 7, line 62 through col. 8, line 11 – the system will continue the process provided while the request inputted into the controller is present, the concurrent data transfer will not conclude until the request no longer exists (i.e. completion of the READ command)).

Searby does not expressly disclose synchronously writing the synchronous read data into the buffer; however, Stolowitz teaches the synchronous writing of synchronous read data into a buffer as ("Synchronous data transfer can be either in parallel, as in FIG. 2, or serialized by a multiplexer… in the read direction, the striped data from the drive is merged on the fly into a single contiguous stream for the cache… Accessing the cache or RAM buffer 106 with a contiguous stream… has the further advantage of... obtaining higher bandwidth at lower cost" (col. 11, lines 1-24) wherein "the control system 640 is arranged to execute synchronous, multiplexed data transfer between the memory buffer 106 and the ring 616 by serially shifting data around the ring" (fig. 6 and related text)).

Searby and Stolowitz are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method/system of reading data from disk drives wherein data is read into a register/buffer as taught by Searby to do so by synchronously writing the synchronous read data into the buffer in the manner taught by Stolowitz since Stolowitz suggests doing so would provide the advantages of "obtaining higher bandwidth at lower cost" (col. 11, lines 1-24).

Therefore, it would have been obvious to combine Searby with Stolowitz for the benefit of creating a method/system to obtain the invention as specified in claims 1 and 10.

As for claim 2, Stolowitz teaches the stored data includes as including user data as well as redundant data sufficient to enable reconstruction of all of the user data in the event of a failure of any single drive of the array and the method further comprising, in the event that one of the disk drives fails, executing said initiating, monitoring, waiting and synchronously reading steps only with respect to the non-failed drives; and dynamically regenerating missing data corresponding to the failed drive from the synchronous read data (col. 8, lines 25-65 – once a drive fails, the system can reconstruct the lost data, and continue to perform the necessary step for data transfer by excluding the drive that failed).

As for claim 3, Searby teaches the method of reading stored data from an array according to claim 1 wherein each two-port memory comprises a FIFO memory (data is written in and out sequentially (i.e. the buffers are used to “buffer” data streamed sequentially – i.e. video data - col. 1, lines 7-29), hence the buffer RAMs act as FIFOs).

As for claim 4, Searby teaches the method of reading stored data from an array according to claim 3 wherein the array comprises a redundant array (col. 3, lines 29-37).

As for claim 5, Searby the method of reading stored data from an array according to claim 4 and further comprising, in the event that one of the disk drives of the redundant array has failed, dynamically regenerating missing data corresponding to the failed drive from the synchronous read data (col. 9, lines 1-39 – parity data is generated and used to replace data in case of a failure).

As for claim 8, Searby teaches the method of reading data from an array according to claim 1 wherein said synchronously reading the stored data from all of the two-port memories comprises asserting a common read enable signal to each of the memories (referring to Fig. 2, the controller (51) asserts the common command line (54) for all RAM buffers to read data from the disk stores).

As for claim 9, though Searby teaches the method of reading data from an array according to claim 1, he fails to teach wherein said synchronously reading the stored data from all of the two-port memories is conducted over a single DMA channel.

Stolowitz however teaches a disk array controller that synchronously transfers data between data port and a buffer memory, which uses a single DMA channel to interface between the drives and the memories (col. 11, lines 5-24).

As for claim 11, Searby teaches the method of reading stored data according to claim 10 wherein the stored data is word striped over the redundant array (col. 4, lines 11-20 and col. 6, lines 14-34 discuss how frames are stored sequentially and striped across each drive. Additionally note the frames are grouped as data words, hence the frames are word striped across the array of disks).

As for claim 12, Searby teaches a method of reading stored data according to claim 10 and further comprising, in the event that one of the disk drives fails to transfer read data to its associated FIFO memory, regenerating the missing read data "on the fly" from the synchronous read data (col. 9, lines 24-60 – the when a error is detected, generated parity information is used account for the error. More specifically, the data regenerator (i.e. data circuitry) performs the bit-wise XOR operation to regenerate missing data due to the drive failure).

As for claim 14, Searby teaches the method of reading data according to claim 10 wherein the synchronous transfer of read data into the common buffer is implemented with a single address counter and a common FIFO read enable signal (referring to Fig. 2, the controller (51) asserts the common command line (54) for all RAM buffers to read data from the disk stores – Additionally, Searby teaches the controller itself as being responsible for generating and counting the addressing to each of the RAM buffers – see Fig. 2).

As for claim 15, though Searby does not explicitly teach a method of reading data from an array according to claim 10 wherein each synchronous transfer of read data into the common buffer stores 64-bits of read data, such a limitation is merely a matter of design choice and would have been obvious in the system of Searby. More specifically, Searby teaches his register (Fig. 2, element 50) as storing information 8-bit format rather than 64-bit as claimed by Applicant. The fact that Searby differs by the claimed invention only by the width of the data stored fails to define a patentably distinct invention over Searby, since both the claimed invention and Searby's teachings are both directed synchronous data transfer from asynchronous devices.

As for claim 16, Searby teaches a method of reading data from an array according to claim 10 and further comprising providing a FIFO memory in the data path between the

individual drive FIFO memories and the common buffer (Fig. 2, elements 4144 depict FIFO buffers between the buffer RAM and the common buffer (50)).

As for claim 17, Searby teaches an improved RAID disk array controller comprising:

a plurality of disk drive interfaces for attaching physical disk drives (Fig. 2 elements 33-36);

a corresponding a two-port memory associated with each of the disk drive interfaces (Fig. 2, elements 37-40 – as discussed with claims 1 and 10, the RAM buffers are FIFO in nature and can be dual-port), each two-port memory arranged to store read data provided by the associated disk drive in a disk read operation and, conversely, to provide write data that was previously-stored in the memory to the associated disk drive in a disk write operation, <u>wherein for each of the disk drives, the disk drive provides a timing signal according to which the read data provided by the disk drive is transferred into the drive's corresponding two-port memory</u> (With respect to this limitation, Searby discloses col. 3, lines 52-67 – data is transferred from the disk stores to the RAM buffers. Conversely, the RAMs may write data to the disk store (col. 5, lines 50-62 – this operation may be reversed to allow the RAMs to write to the disk stores) and explains, “individual sub-controllers… between each of the second SCSI interfaces 33 and 36 and their respective RAM buffer 37 to 40. Each sub-controller would monitor the request signal REQ from its second SCSI interface and in response to a request would strobe the write line of its RAM buffer causing a word to be transferred from the second SCSI interface to the RAM buffer” (col. 7, lines 14-20), describing the embodiment depicted in fig. 2 as "disc drives and associated circuitry” (col. 7, lines 60-61); *where Applicant*

should note that SCSIs and the disclosed sub-controllers are associated with each of the disk drives and may thus be interpreted as forming part of the disk drives (Refer to Board decision, page 11, lines 1-12); therefore, having the disk drives provide the timing signals. Further, it would have been obvious to one having ordinary skill in the art to place the disk and associated circuitry (i.e., SCSI and sub-controller) as disclosed by Searby within the same chip or drive, since relocation or rearrangement of parts is an obvious matter to one having ordinary skill in the art. In re Japikse, 86 USPQ 70););

a logic circuit coupled to all of the two-port memories for detecting when all of the two-port memories have data stored therein for a read operation or available space therein for a write operation (col. 7, lines 32-46 – the system transfers the data to the data highway (Fig. 2, element 49) based on the determination that data is stored in the RAM buffers. Since all the buffers receive data substantially concurrently (i.e. all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e. non-empty condition), or not present. Data present in the RAM buffers is an implied acknowledgment that data have been received from the disk stores. Note the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur (his operation is controlled by the controller (i.e. logic circuit) which is coupled to the RAMs));

control circuitry responsive to the logic circuit for synchronously reading data from all of the two-port memories only when all of the two-port memories have data

stored therein, thereby forming synchronous read data (col. 7,lines 32-35 – once all RAMs indicate a non-empty condition (i.e. data is present in each RAM), the data is sent to the data highway and subsequently to the register (i.e. buffer) as shown in Fig. 2, element 50 (see also col. 5, lines 22-37 and col. 6, lines 14-31)). Again, the RAM buffers store data such that either all contain data, or no buffers contain data, therefore the data cannot be transferred until all RAM buffers have data (i.e. are non-empty). The controller, via the aid of SCSI interface logic; controls this function;

the control circuitry further responsive to the logic circuit for detecting that all of the two-port memories have space therein and synchronously writing data to all of the two port memories thereby forming synchronous write data (the system will continue to buffer the data if it is determined that space is available to stream more data (col. 7, line 62 through col. 8, line 11));

first redundant data circuitry for regenerating missing data "on the fly" from the synchronous read data in the event that one of the disk drives fails to provide read data to its associated two-port memory in a read operation (col. 9, lines 24-60 – the when a error is detected, generated parity information is used account for the error. More specifically, the data regenerator (i.e. data circuitry) performs the bit-wise XOR operation to regenerate missing data due to the drive failure); and

second redundant data circuitry for generating redundant data "on the fly" from the synchronous write data for storing in the array (col. 9, lines 1-39 – the last drive of the array is used to store parity information. In case of a drive failure, the data in this last

disk store can be used to generate the data needed to correct the drive failure) and wherein:

Searby however fails to teach one of the disk interfaces as being specifically connected to a redundant disk wherein the first redundant circuitry regenerates corrected in the event of a failed drive without delaying the output of the read data, and synchronously transferring the read data to a common buffer as recited by Applicant in the instant claim.

Stolowitz however teaches a disk array controller including:

one of the disk drive interfaces is designated for connection to a redundant disk drive for storing redundant data so that the synchronous read data includes redundant data (col. 13, line 55 through col. 14, line 3 – the drives include a redundant drive) ;

the first redundant data circuitry for regenerating missing data is coupled to all of the memories to receive the synchronous read data, including the redundant data, and further is arranged to compute a redundant data operation across the synchronous read data so as to provide corrected data in the event of a failed drive without delaying output of the read data (col. 8, lines 25-65 – once a drive fails, the system can reconstruct the lost data, and continue to perform the necessary step for data transfer by excluding the drive that failed. Note Stolowitz explicitly teaches no delay occurring during this process)

and the synchronous writing of synchronous read data into a buffer as ("Synchronous data transfer can be either in parallel, as in FIG. 2, or serialized by a multiplexer… in the read direction, the striped data from the drive is merged on the fly into a single contiguous stream for the cache… Accessing the cache or RAM buffer 106 with a contiguous stream… has the further

advantage of... obtaining higher bandwidth at lower cost" (col. 11, lines 1-24) wherein "the control system 640 is arranged to execute synchronous, multiplexed data transfer between the memory buffer 106 and the ring 616 by serially shifting data around the ring" (fig. 6 and related text)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Searby to further include Stolowitz's disk array controller and method to synchronously transfer data into his own system of synchronously transferring data. By doing so, Searby would benefit by improving his own disk array performance and improve his disk array storage reliability while reducing the cost and complexity of his present controller to perform a synchronous data transfer as taught by Stolowitz (col. 6, lines 4-18), where, it would have further been obvious to modify the method/system of reading data from disk drives wherein data is read into a register/buffer as taught by Searby to do so by synchronously writing the synchronous read data into the buffer in the manner taught by Stolowitz since Stolowitz suggests doing so would provide the advantages of "obtaining higher bandwidth at lower cost" (col. 11, lines 1-24).

As for claim 19, Searby teaches an improved RAID disk array controller according to claim 17 wherein each two-port memory comprises a FIFO memory data is written in and out sequentially (i.e. the buffers are used to "buffer" data streamed sequentially – i.e. video data - col. 1, lines 7-29, the buffer RAMs act as FIFOs).

As for claim 20, Stolowitz teaches a buffer comprising DRAM (Fig. 6, element 106).

As for claim 21, Searby teaches an improved RAID disk array controller according to claim 17 and further comprising a single address counter arranged for addressing the buffer for transfers between the buffer and the FIFO memories in either direction (the controller itself is

responsible for generating and counting the addressing to each of the RAM buffers – see Fig. 2 – Additionally note the data transfer can occur either from disk stores to the RAM buffers or vise versa – col. 5, lines 50-62).

As for claims 22-23, Stolowitz teaches all drives implement a ATA/ATAPI interface (Fig. 2, all drives are IDE – Stolowitz discusses the equivalence of IDE and ATA – col. 4, lines 1-10). Note this similar comparison is discussed in Applicant's original specification paragraph 0005.

As for claim 24, Stolowitz teaches the array controller as being implemented on a signal motherboard (col. 13, line 57 through col. 14, line 3).

As for claim 25, Stolowitz teaches the array controller as being implemented on a Host Bus Adapter (Fig. 2, element 104 - since a host bus adapter is defined as "a device for connecting a peripheral to the main computer", the host interface serves as a host bus adapter as it interfaces the array controller and disks with the host itself via the host bus (Fig. 2, element 102)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Searby to further include Stolowitz's disk array controller and method to synchronously transfer data into his own system of synchronously transferring data. By doing so, Searby would benefit by improving his own disk array performance and improve his disk array storage reliability while reducing the cost and complexity of his present controller to perform a synchronous data transfer as taught by Stolowitz (col. 6, lines 4-18).

Claims 6, 7, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186) and Stolowitz (US Patent 6,018,778) as applied to claims 1 and 10 above, and in further view of Anderson (US PG Publication 2003/0200478 A1)

As for claims 6, 7, and 13, though Searby teaches all the limitations of claims 1,10, and 26, he failures to teach the read operation as being effected via corresponding UDMA interface to each of the disk drives (or coupled to each of the drives via the UDMA interface as recited in claim 13).

Anderson however teaches a media server with single chip storage controller, which includes a plurality of storage devices (Fig. 2, element 10, interfaced with a controller (12) over a plurality of communication lines (14). Note Anderson specifically teaches the communication lines as being UDMA interfaces (paragraph 0101, all lines)).

It would have been obvious for Searby to further include Anderson's single chip storage controller into his own system for synchronous data transfer. By doing so, Searby would benefit by having a more efficient RAID storage controller which is integrated to enable rapid recovery from failures as taught by Anderson in paragraph 0006, all lines. Anderson specifically advises the application of this benefit to systems such as Searby's, which processes video data. Searby would additionally benefit from Anderson's reduction of unwanted interruption by enabling hot swapping of failed drives as taught by Anderson in paragraphs 0016 and 0017, all lines.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Searby (US Patent 5,765,186) and Stolowitz (US Patent 6,018,778) as applied to claim 17 above, and in further view of Yamamoto (US Patent 5,801,859).

As for claim 18, though the combined teachings of Searby and Stolowitz disclose, allowing the dual port memory to transfer data in either direction via unique I/O ports, they fail to teach exchanging them via multiplexers as claimed by Applicant. Yamamoto however teaches a network system for plural node devices without arbitration, in which the port (either input or output) can be exchanged via multiplexing logic (col. 30, lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Searby and Stolowitz to further include Yamamoto's system into his own system for synchronously transferring data. By doing so, they would benefit by having a more efficient means of data transfer while preventing the need for increased hardware costs as taught by Yamamoto in col. 5, lines 51-67.

Claims 26-28, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186).

As for claim 26, Searby teaches a method of writing data into an array of independent disk drives, the method comprising:

providing a buffer for storing write data (Fig. 2, element 50);

for each disk drive in the array, providing a corresponding two-port memory for receiving and storing write data (Fig. 2, elements 37-40 – the RAM buffers are dual-port as described in the rejection of claim 1);

monitoring each of the two-port memories to detect a non-full condition (col. 7, lines 32-46 – the system transfers the data to the data highway (Fig. 2, element 49) based on the determination that data is stored in the RAM buffers. Since all the buffers receive data substantially concurrently (i.e. all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e. non-empty condition), or not present. Note the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur);

waiting until all of the two-port memories indicate such a non-full condition; then reading write data from the buffer (again the data is read out of the buffer only when data is present in the buffers. The system must detect that data has been written to the RAM buffers before it can transfer data from each of the RAM buffers to the buffer);

computing redundant data from said write data (col. 9, lines 24-59 – redundant data is calculated base on the information in the buffer);

synchronously storing the write data and the computed redundant data into the two-port memories via a first port of each two-port memory (the parity data and the data

to be written are stored concurrently, and are stored via the first port of the dual-port memory – col. 9, lines 24-59); and

while synchronously storing the write data and the computed redundant data into the two-port memories, transferring stored data from a second port of each of the two-port memories into its corresponding disk drive, in each case transferring the previously-stored data responsive to timing control provided by the corresponding disk drive, wherein for each of the disk drives, the disk drive provides the timing control according to which the previously-stored data is transferred into the disk drive (With respect to this limitation, Searby discloses the controller is responsible for asserting the control signal to enable access for writing to and from each buffer RAM simultaneously. Col. 5, lines 50-62, the data can be either written to or from the RAM buffers and disk stores. The memory is dual-port which permits the system to uniquely assign the functions each of the two ports, and explains "this function of the controller 51 could, if desired, be realized by individual sub-controllers… between each of the second SCSI interfaces 33 and 36 and their respective RAM buffer 37 to 40. Each sub-controller would… strobe the write line of its RAM buffer causing a word to be transferred from the second SCSI interface to the RAM buffer" (col. 7, lines 14-20) where in col. 5, lines 50-62, Searby explains the write operation to write data in the disks as substantially the reverse of the reading, describing the embodiment depicted in fig. 2 as "disc drives and associated circuitry" (col. 7, lines 60-61); *where Applicant should note that SCSIs and the disclosed sub-controllers are associated with each of the disk drives and may thus be interpreted as forming part of the disk drives (Refer to Board decision, page 11, lines 1-12); therefore,*

having the disk drives provide the timing signals. Further, it would have been obvious to one having ordinary skill in the art to place the disk and associated circuitry (i.e., SCSI and sub-controller) as disclosed by Searby within the same chip or drive, since relocation or rearrangement of parts is an obvious matter to one having ordinary skill in the art. In re Japikse, 86 USPQ 70);

As for claim 27, Searby teaches a method of writing data into an array according to claim 26 and further comprising stalling said storing step whenever any of the two-port memories become full, but only with regard to the full memory, while allowing said synchronously storing the write data to continue into the non-full two-port memories (data storage will continue without delay provided the system recognizes that enough free memory is available in the buffer RAM devices – col. 8, lines 1-11).

As for claim 28, Searby teaches a method of writing data into an array according to claim 27 wherein each two-port memory comprises a FIFO memory (data is written in and out sequentially (i.e. the buffers are used to "buffer" data streamed sequentially – i.e. video data - col. 1, lines 7-29), the buffer RAMs act as FIFOs).

As for claim 31, Searby teaches a method of storing data into an array according to claim 28 wherein said synchronously storing the write data into the FIFOs comprises asserting a common write strobe coupled to all of the FIFO memories (referring to Fig. 2, the controller (51) asserts the common command line (54) for all RAM buffers to read data from the disk stores).

Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186) as applied to claim 26 above and in further view of Anderson (US PG Publication 2003/0200478 A1)

As per claims 29, and 30, though Searby teaches all the limitations of claims 1,10, and 26, he failures to teach the read operation as being effected via corresponding UDMA interface to each of the disk drives (or coupled to each of the drives via the UDMA interface as recited in claim 13).

Anderson however teaches a media server with single chip storage controller, which includes a plurality of storage devices (Fig. 2, element 10, interfaced with a controller (12) over a plurality of communication lines (14). Note Anderson specifically teaches the communication lines as being UDMA interfaces (paragraph 0101, all lines)).

It would have been obvious for Searby to further include Anderson's single chip storage controller into his own system for synchronous data transfer. By doing so, Searby would benefit by having a more efficient RAID storage controller which is integrated to enable rapid recovery from failures as taught by Anderson in paragraph 0006, all lines. Anderson specifically advises the application of this benefit to systems such as Searby's, which processes video data. Searby would additionally benefit from Anderson's reduction of unwanted interruption by enabling hot swapping of failed drives as taught by Anderson in paragraphs 0016 and 0017, all lines.

<u>ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT</u>

Response to Amendment

4. Applicant's arguments filed on 2/17/2010 have been considered but are moot in view of the new ground(s) of rejection. However, some of Applicant's arguments regarding Searby are deemed to not overcome obviousness in view of the reference.

5. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

6. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

7. Applicant argues Searby does not disclose wherein for each of the drives, the drive provides one of the timing signals.

8. In response, these arguments have been fully considered but are not deemed persuasive since Searby discloses col. 5, lines 38-49; col. 7, lines 12-26 – the control bus is used to in conjunction with request signals (REQ) to indicated a READ command – i.e. when data is to be read from the drives to the RAM buffers, and explains "individual sub-controllers… between each of the second SCSI interfaces 33 and 36 and their respective RAM buffer 37 to 40. Each sub-controller would… strobe the write line of its RAM buffer causing a word to be transferred from the second SCSI interface to the RAM buffer" (col. 7, lines 14-20), wherein in col. 5, lines 50-62, Searby explains that the write operation would be substantially the inverse of the read; thus the teachings of the invention would also apply to writing data into disks, describing the embodiment depicted in fig. 2 as "disc drives and associated circuitry" (col. 7, lines 60-61);

where Applicant should note that SCSIs and the disclosed sub-controllers are associated with each of the disk drives and may thus be interpreted as forming part of the disk drives (Refer to Board decision, page 11, lines 1-12); therefore, having the disk drives provide the timing signals. Further, it would have been obvious to one having ordinary skill in the art to place the disk and associated circuitry (i.e., SCSI and sub-controller) as disclosed by Searby within the same chip or drive, since relocation or rearrangement of parts is an obvious matter to one having ordinary skill in the art. In re Japikse, 86 USPQ 70.

9. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant’s response that was traversed, rendered moot or found persuasive above.

10. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated 2/17/2010.

CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

11. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) <u>CLAIMS REJECTED IN THE APPLICATION</u>

12. Per the instant office action, claims 1-31 have received a first action on the merits and are subject of a non-final rejection.

b. <u>DIRECTION OF FUTURE CORRESPONDENCES</u>

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232, and email address is yaima.campos@uspto.gov . The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

14. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 26, 2010

/Yaima Campos/
Examiner, Art Unit 2185